AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) ~~Method~~ A method for processing an input bit sequence in a digital communication system, said method including the steps of:

a) storing ~~(66)~~ the bits of said input bit sequence at locations of a memory means indicated by a first interleaving scheme,

b) converting ~~(69)~~ output bit positions into input bit positions according to an inverse of a second interleaving scheme,

c) reading out ~~(73)~~ bits stored at locations of said memory means corresponding to said input bit positions, thereby generating an interleaved sequence which is interleaved according to said first and said second interleaving schemes,

d) processing ~~(74)~~ said interleaved sequence according to further physical processing steps, wherein the execution periods of the converting and processing steps overlap in time.

2. (Currently Amended) A method ~~Method~~ for processing an input bit sequence in a digital communication system, said method including the steps of:

a) storing the bits of said input bit sequence in a memory means,

b) converting output bit positions into input bit positions according to an inverse of a sequential application of a first interleaving scheme and a second interleaving scheme,

c) reading out bits stored at locations of said memory means corresponding to said input bit positions, thereby generating an interleaved sequence which is interleaved according to said first and said second interleaving schemes,

d) processing said interleaved sequence according to further physical processing steps, wherein the execution periods of the converting and processing steps overlap in time.

3. (Currently amended) The method ~~Method~~ according to claim ~~1 or~~ 2, wherein execution periods of the converting and processing steps ~~are executed in~~ overlap in time ~~essentially the same period of time~~.

4. (Currently Amended) The method ~~Method~~ according to claim 2 ~~one of the claims 1 to 3~~, wherein the execution periods of the converting and storing steps overlap in time.

5. (Currently Amended) The method ~~Method~~ according to claim 2 ~~one of the claims 1 to 4~~, wherein said reading step begins upon completion of ~~adapted to begin with its operations at the earliest possible instant in time after~~ said storing step ~~has finished its operations~~.

6. (Currently Amended) The method ~~Method~~ according to claim 2 ~~one of the claims 1 to 5~~, wherein said further physical processing steps further include a step of modulation.

7. (Currently Amended) The method ~~Method~~ according to claim 2 ~~one of the claims 1 to 6~~, wherein said further physical processing steps further include ~~a~~ step of spreading.

8. (Canceled)

9. (Currently Amended) Apparatus for processing an input bit sequence in a digital communication system, including:

a) a memory means ~~(75)~~ capable of storing said input bit sequence,

b) a first processing unit ~~(76)~~ adapted to store the bits of said input bit sequence at locations of said memory means indicated by a first interleaving scheme,

c) a second processing unit ~~(77,78)~~ adapted to:

convert output bit positions into input bit positions according to an inverse of a second interleaving scheme,

read out bits being stored at locations of said memory means corresponding to said input bit positions, thereby generating an interleaved sequence which is interleaved according to said first and said second interleaving schemes, and

process said interleaved sequence ~~according to further physical processing steps, wherein the second processing unit is adapted~~ to convert bit positions and to process said interleaved sequence in overlapping periods of time.

10. (Currently Amended) An apparatus ~~Apparatus~~ for processing an input bit sequence in a digital communication system, including:

a) a memory means capable of storing said input bit sequence,

b) a first processing unit adapted to store the bits of said input bit sequence in said memory means, and

c) a second processing unit adapted to:

convert output bit positions into input bit positions according to an inverse of a sequential application of a first interleaving scheme and a second interleaving scheme,

read out bits stored at locations of said memory means corresponding to said input bit positions, thereby generating an interleaved sequence which is interleaved according to said first and said second interleaving schemes~~,~~

process said interleaved sequence ~~according to further physical processing steps, wherein the second processing unit is adapted~~ to convert bit positions and to process said interleaved sequence in overlapping periods of time.

11. (Currently Amended) The apparatus ~~Apparatus~~ according to claim ~~9~~ ~~or~~ 10, wherein the second processing unit is adapted to convert bit positions and to process said interleaved sequence in ~~essentially~~ the same period of time.

12. (Currently Amended) The apparatus ~~Apparatus~~ according to claim 10 ~~one of the claims 9 to 11~~ adapted to convert bit positions and to store the bits of said input bit sequence in overlapping periods of time.

13. (Currently Amended) The apparatus ~~Apparatus~~ according to claim 10 ~~one of the claims 9 to 12~~ adapted to begin ~~with~~ reading operations upon completion of ~~at the earliest possible instant in time after having finished~~ the storing operations.

14. (Currently Amended) The apparatus ~~Apparatus~~ according to claim 10 ~~one of the claims 9 to 13~~, wherein said further physical processing steps include a step of modulation.

15. (Currently Amended) The apparatus ~~Apparatus~~ according to claim 10 ~~one of the claims 9 to 11~~, wherein said further physical processing steps include a step of spreading.

16. (New) The method according to claim 1, wherein the converting and processing steps are executed in the same period of time.

17. (New) The method according to claim 1, wherein the execution periods of the converting and storing steps overlap in time.

18. (New) The method according to claim 1, wherein said reading step commences operations following completion of said storing step.

19. (New) The method according to claim 1, wherein said further physical processing steps include a step of modulation.

20. (Previously Presented) The method according to claim 1, wherein said further physical processing steps include a step of spreading.

21. (New) The apparatus according to claim 9, wherein the second processing unit is adapted to convert bit positions and to process said interleaved sequence in the same period of time.

22. (New) The apparatus according to claim 9 adapted to convert bit positions and to store the bits of said input bit sequence in overlapping periods of time.

23. (New) The apparatus according to claim 9 adapted to beginning reading operations following completion of the storing operations.

24. (New) The apparatus according to claim 9, wherein said further physical processing steps include a step of modulation.

25. (New) The apparatus according to claim 9, wherein said further physical processing steps include a step of spreading.